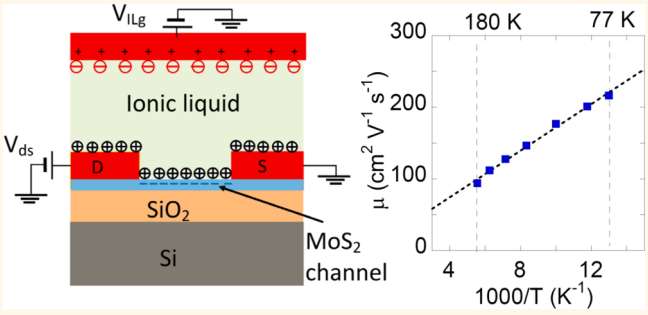
Improved Carrier Mobility in Few-Layer MoS_2 Field-Effect Transistors with Ionic-Liquid Gating

Meeghage Madusanka Perera,[†] Ming-Wei Lin,[†] Hsun-Jen Chuang,[†] Bhim Prasad Chamlagain,[†] Chongyu Wang,[†] Xuebin Tan,[‡] Mark Ming-Cheng Cheng,[‡] David Tománek,[§] and Zhixian Zhou[†,*]

[†]Department of Physics and Astronomy, Wayne State University, Detroit, Michigan 48201, United States, [‡]Department of Electrical and Computer Engineering, Wayne State University, Detroit, Michigan 48202, United States, and [§]Physics and Astronomy Department, Michigan State University, East Lansing, Michigan 48824, United States

ABSTRACT We report the fabrication of ionic liquid (IL)-gated field-effect transistors (FETs) consisting of bilayer and few-layer MoS_2. Our transport measurements indicate that the electron mobility $\mu \approx 60$ cm^2 V^{-1} s^{-1} at 250 K in IL-gated devices exceeds significantly that of comparable back-gated devices. IL-FETs display a mobility increase from ≈100 cm^2 V^{-1} s^{-1} at 180 K to ≈220 cm^2 V^{-1} s^{-1} at 77 K in good agreement with the true channel mobility determined from four-terminal measurements, ambipolar behavior with a high ON/OFF ratio >10^7 (10^4) for electrons (holes), and a near ideal subthreshold swing of ≈50 mV/dec at 250 K. We attribute the observed performance enhancement, specifically the increased carrier mobility that is limited by phonons, to the reduction of the Schottky barrier at the source and drain electrode by band bending caused by the ultrathin IL dielectric layer.



KEYWORDS: field-effect transistor · MoS_2 · few-layer · electric double layer · Schottky barrier

In the quest for flexible electronics in the "post-silicon" era, graphene has attracted much attention due to unsurpassed carrier mobility and high thermal conductivity,[1−4] combined with excellent chemical and thermal stability down to the nanometer scale.[5] The major drawback is the absence of fundamental band gap, which makes semimetallic graphene unsuitable for conventional digital logic applications. Sustained efforts to engineer a band gap in graphene have either caused severe mobility degradation or require prohibitively high bias voltages.[6−9]

Molybdenum disulfide (MoS_2), a layered transition-metal dichalcogenide (TMD), has emerged as a viable alternative to graphene, as it combines a semiconducting gap with mechanical flexibility, chemical and thermal stability and absence of dangling bonds. The single-layer MoS_2 consists of a molybdenum monolayer sandwiched between two sulfur monolayers. The fundamental band gap changes from an ≈1.2 eV wide indirect gap in the bulk to a direct gap of ≈1.8 eV in single-layer MoS_2.[10,11] Similar to graphene, single MoS_2 layers can be extracted from bulk crystals by a mechanical cleavage technique due to relatively weak interlayer interaction with an important van der Waals character.[12] Besides conventional field effect transistors (FETs), the use of MoS_2 has been proposed for applications such as energy harvesting[13,14] and optoelectronics.[15,16] Recently, integrated circuits based on MoS_2 transistors have also been demonstrated, which is a significant step toward the application of MoS_2 in high-performance low-power nanoelectronics.[17] However, the room temperature carrier mobility in single- and few-layer MoS_2 FETs fabricated on Si/SiO_2 substrates was found to be very low, typically in the range of 0.1 −10 cm^2 V^{-1} s^{-1}.[12,17,21] This mobility is not only orders of magnitude lower than that of graphene, but also substantially lower than the phonon-limited mobility in the bulk system,[12,18−21] which is of the order of 100 cm^2 V^{-1} s^{-1}. The interface between the MoS_2 channel and the SiO_2 gate

* Address correspondence to zxzhou@wayne.edu.

Received for review March 1, 2013 and accepted April 16, 2013.

Published online April 16, 2013
10.1021/nn401053g

dielectric has been considered as one of the primary factors limiting carrier mobility.[18] A substantial mobility enhancement to over 200 $cm^2 V^{-1} s^{-1}$ and 500 $cm^2 V^{-1} s^{-1}$ has been reported for HfO_2 and Al_2O_3 capped monolayer and multilayer MoS_2 FETs, respectively, which was attributed to high-κ dielectric screening of charged impurities that reduces scattering at the channel/dielectric interface.[22,23] There are also rising concerns that the mobility in these devices might have been substantially overestimated.[24]

For large band gap semiconductors such as MoS_2, a significant Schottky barrier may form at the metal/semiconductor contact, yielding a high contact resistance.[10,25] Lee *et al.* showed in their study of MoS_2 flakes produced by liquid exfoliation that the mobility in MoS_2 FETs could be largely underestimated due to the Schottky barriers at the MoS_2/metal contacts.[26] In the presence of a substantial Schottky barrier, the extrinsic mobility is also expected to degrade with decreasing temperature due to the reduced thermionic emission current and thermally assisted tunneling current, as was recently observed by Ghatak *et al.* in atomically thin MoS_2 FETs.[18] In agreement with recent predictions,[24] Das *et al.* has demonstrated a significant mobility enhancement by reducing the Schottky barrier height using a low work function contact metal, which further indicates that the performance of MoS_2 FETs can be strongly influenced by the metal/semiconductor contacts.[26]

To optimize the performance of MoS_2 FETs, it is crucial to use low resistance Ohmic contacts. There are typically two types of low resistance contacts that can be made between a semiconductor and a metal: (a) Schottky contacts with a very low barrier height and (b) highly transparent tunneling contacts. Ideally, an Ohmic contact can be formed if the Schottky barrier height is zero (or negative). Contacts with low Schottky barrier height ($\approx$30 meV) have been achieved in multilayer MoS_2 by using Scandium as a low work function contact metal.[27] However, the tunability of the Schottky barrier height may be reduced by Fermi level pinning.[21] Alternatively, highly transparent tunneling contacts can be fabricated by heavily doping the semiconductor in the contact region. This approach fails for MoS_2, because ionized impurity doping would substantially damage the structural integrity of the atomically thin channel. As an alternative, surface doping with strongly oxidizing NO_2 molecules has been used to narrow the Schottky barrier thickness for hole injection and thus reduce the contact resistance of WSe_2 FETs.[28]

In this article, we report electrostatic doping using an ionic-liquid (IL) gate as a viable approach to achieve low resistance MoS_2/metal tunneling contacts. We demonstrate (i) significant improvement in the performance of few-layer MoS_2 FETs and (ii) high carrier mobility in the MoS_2 channel that is limited by phonons. ILs are binary organic salts that can form electric double layers at the IL/solid interface and thus act as nanogap capacitors with extremely large capacitance. As we show in the following, the Schottky barrier can be drastically reduced in IL-gated FETs (IL-FETs) of MoS_2. We observe a significant increase of the tunneling efficiency that can be attributed to strong band bending at the MoS_2/metal interface, provided by the thin electrical double layer with a high capacitance. As a result, our nanometer-thick MoS_2 IL-FETs exhibit a significantly enhanced extrinsic mobility that exceeds 60 $cm^2 V^{-1} s^{-1}$ at 250 K, in contrast to $\mu < 5$ $cm^2 V^{-1} s^{-1}$ measured in the Si-back-gate configuration without IL. The MoS_2 IL-FETs further exhibit ambipolar behavior with a high current ON/OFF ratio exceeding 10^7 for electrons and 10^4 for holes, and a near ideal subthreshold swing (SS) of $\sim$50 mV/decade at 250 K. More significantly, the mobility in few-layer MoS_2 IL-FETs increases from $\sim$100 $cm^2 V^{-1} s^{-1}$ to $\sim$220 $cm^2 V^{-1} s^{-1}$ as the temperature decreases from 180 to 77 K, which is in good agreement with the true channel mobility derived from our four-terminal measurements. The temperature dependence of the mobility behaves as $\mu \sim T^{-\gamma}$ with $\gamma \approx 1$, indicating that the mobility is predominantly limited by phonon scattering in this case.

RESULTS AND DISCUSSION

Atomically thin MoS_2 flakes were produced from a bulk crystal by a mechanical cleavage method and subsequently transferred onto degenerately doped silicon substrates covered with a 290 nm thick thermal oxide layer.[12,29] An optical microscope was used to identify thin flakes, which were further characterized by noncontact mode atomic force microscopy (AFM). In the present study, we focus on bilayer and few-layer (2−7 layers corresponding to 1.3−5 nm thickness) samples, because the yield of bilayer and few-layer flakes was found to be much higher than that of single-layer MoS_2. Moreover, few-layer MoS_2 also tends to form lower Schottky barriers (thus, smaller contact resistance) than single-layer samples.[21,27] MoS_2 IL-FET devices were fabricated by first patterning the source, drain and gate electrodes, consisting of 5 nm of Ti covered by 50 nm of Au, using standard electron beam lithography and electron beam deposition.[8] A small droplet of the DEME-TFSI IL (Sigma Aldrich 727679) was then carefully applied onto the devices using a micromanipulator under an optical microscope, covering the MoS_2 layer and the source, drain, and gate electrodes.[30] The IL gate forms by self-assembly. DEME-TFSI has been chosen for its large electrochemical stability window (>3 V at room temperature).

Figure 1a shows a micrograph and Figure 1b shows the schematic of a typical IL-gated MoS_2 device. Electrical properties of the devices were measured by a Keithley 4200 semiconductor parameter analyzer in a Lakeshore Cryogenic probe station after dehydrating the IL under high vacuum ($\sim 1 \times 10^{-6}$ Torr) for 48 h.

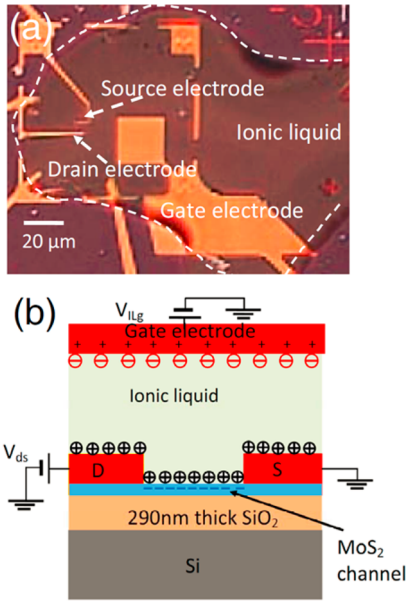


Figure 1. (a) Optical micrograph of a typical IL-gated MoS_2 FET. The contour of the IL drop covering the MoS_2 channel and the in-plane gate-electrode are marked by white dotted lines. The scale bar is 20 μm. (b) Schematic illustration of the working principle of an IL-gated MoS_2 FET.

This thorough removal of the remaining moisture turned out to be important to preventing the formation of chemically reactive protons and hydroxyls through the electrolysis of water.[31] Most measurements on IL-gated devices were carried out at 250 K or below to further reduce the possibility of any chemical reactions between the IL and MoS_2.[32] As shown schematically in Figure 1b, negative ions in the IL accumulate near the gate electrode and positive ions accumulate near the MoS_2 channel when a positive voltage is applied to an IL-gate-electrode near the device channel. The scenario reverses when a negative voltage is applied to the gate. In both cases, electric double layers form at the interfaces between the IL and solid surfaces.[33] To ensure that nearly all of the gate voltage appears as potential drop across the IL/channel interface, the surface area of the gate electrode is 1−2 orders of magnitude larger than the total area of the transport channel plus parts of the drain/source electrodes, which are immersed in the IL.[34] Downscaling of the IL-gated devices can be achieved by simultaneously reducing the surface area of the gate electrode and covering a large part of the drain/source electrodes with an insulating overlayer.[35]

We have measured several IL-gated bilayer and few-layer MoS_2 FETs and observed consistent results. Figure 2 shows the transfer characteristics of two representative devices measured at a drain-source voltage of 1 V. Both the bilayer and trilayer devices exhibit ambipolar behavior, with the current ON/OFF ratio exceeding 10^7 for electrons in both devices. The observed ON/OFF ratio for holes was 10^6 in the bilayer

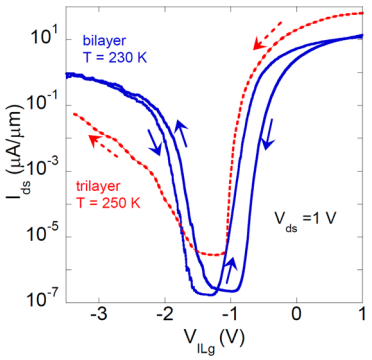


Figure 2. Transfer characteristics of representative bilayer and trilayer MoS_2 IL-gated FETs measured at the drain-source bias V_{ds} = 1 V.

and 10^4 in the trilayer device. Ambipolar behavior has been previously observed in ion-liquid-gated thicker MoS_2 flakes (>10 nm) by Zhang *et al.*[32] However, their ON/OFF ratio was less than 10^3 for both electrons and holes, presumably due to the relatively large "OFF" state current passing through the interior of the crystal beneath the channel surface. This current ON/OFF ratio is much lower than the typical values between 10^4 and 10^7, which are desired for digital logic devices.[22] It is worth pointing out that our observation of hole conduction in bilayer and few-layer MoS_2 is rather surprising in view of the large Schottky barrier height (∼1 eV) for the hole-channel.[21] Our results suggest that holes are injected into the MoS_2 channel primarily by thermally assisted tunneling rather than by thermionic emission.[36] The tunneling rate is increased significantly for both electrons and holes in presence of the extremely thin (∼1 nm) dielectric layer formed by the IL gate, which significantly reduces the thickness of Schottky barrier through strong band bending near the contacts at high gate voltages. Because the formation of an electrical double layer on the MoS_2 contacts near the edge of the metal electrodes is conformal, the thickness of the contact Schottky barrier can be reduced very effectively by the IL gate down to the electrostatic screening length in the IL (∼1 nm).[37] The asymmetry between electron and hole transport can be attributed to (1) a larger Schottky barrier height for the hole channel that reduces thermally assisted tunneling, (2) a slight preference for the adsorption of positive ions on MoS_2, as discussed later, and (3) intrinsic *n*-doping of the transport channel. All of these effects tend to favor electron *versus* hole transport, shifting the transfer curves toward the negative gate-voltage direction. The lower asymmetry between electron and hole transport (observed when the gate voltage was swept from positive to negative), causing a more balanced ambipolar character of the bilayer MoS_2 device, may be attributed to a slightly lower degree of intrinsic *n*-doping in the bilayer flake.[34] The hysteresis in the transfer characteristics could be attributed to the charge injection at the interfaces

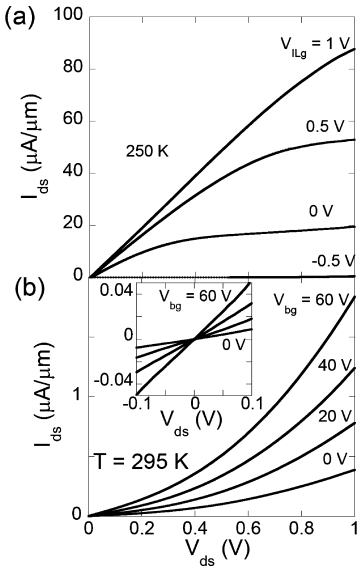


Figure 3. Comparison of the output characteristics of the trilayer MoS_2 device used in Figure 2, measured in the IL-gate and back-gate (without IL) configurations. (a) Drain-source current I_{ds} as a function of the drain-source bias V_{ds} at IL-gate voltages between −0.5 and 1 V. (b) I_{ds} as a function of V_{ds} at selected back-gate voltages between 0 and 60 V before the IL was deposited. The inset in (b) shows the magnified low-bias region in this panel.

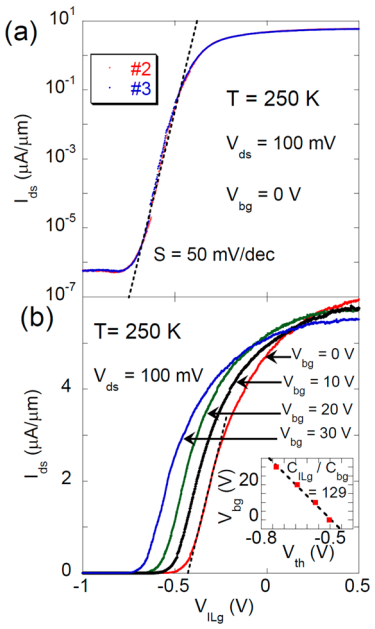


Figure 4. (a) Transfer characteristics of the identical trilayer MoS_2 device in two separate runs, where the IL-gate voltage was swept at V_{ds} = 100 mV, V_{bg} = 0 V, and T = 250 K. (b) Transfer curves of the identical IL-gate device measured at various back-gate voltages between 0 and 30 V. The inset in (b) shows the back-gate voltage *vs* the threshold voltage of the transfer curves.

between the channel and the substrate as well as the slow motion of the ions at low temperature.[32,38]

Low contact resistance is an important prerequisite to realize the full potential of MoS_2 as a channel material for FETs. Because the Schottky barrier for holes is larger than for electrons, the contact resistance in the hole channel is higher than in the electron channel. To optimize the device performance, we next focus on the electron channel only and study the impact of IL-induced Schottky barrier thinning on its electrical characteristics. Figure 3 shows the output characteristics of a trilayer MoS_2 device that was measured both with an IL-gate and a back-gate with no IL present. As shown in Figure 3a, the drain current in the IL-gate voltage range of $0 < V_{ILg} < 1$ V exhibits linear dependence at low drain-source voltages and starts to saturate at higher V_{ds}. The current saturation at high V_{ds} can be attributed to the channel pinch-off of the FET. In sharp contrast to these data, the same device, when measured in the back-gate configuration without IL, exhibits strongly nonlinear (upward turning) $I_{ds}-V_{ds}$ behavior, suggesting the presence of a significant Schottky barrier at the contacts (Figure 3b). Furthermore, the total resistance calculated from the slope of the $I_{ds}-V_{ds}$ characteristics in the low-bias region is over 2 orders of magnitude larger for the Si back-gate configuration (2×10^6 Ω at V_{bg} = 60 V, see the inset of Figure 3b) than for the IL-gate configuration (1×10^4 Ω at V_{ILg} = 1 V), providing further evidence that IL gating significantly reduces the contact resistance by thinning the Schottky barrier. Note that linear $I_{ds}-V_{ds}$ dependence at small bias voltages ($V_{ds} < 0.1$ V, shown in the inset of Figure 3b) is only a necessary, but not a sufficient condition for a low-resistance Ohmic contact. Linear current−voltage behavior may also be due to the thermally assisted tunneling current, especially at small drain-source voltages.[27]

The observed drastic reduction of the contact resistance by IL gating opens up the possibility of investigating channel-limited device parameters in nanometer-thick MoS_2 devices. Figure 4a shows the transfer characteristics from two separate measurements of the same trilayer MoS_2 device at T = 250 K, for V_{ds} = 0.1 V and V_{bg} = 0 V. The high reproducibility of the transfer curves indicate that charged ions in the IL are electrostatically accumulated at the gate/electrolyte and MoS_2/electrolyte interfaces without any noticeable chemical reactions. The transfer characteristics also remain essentially unchanged at different gate voltage sweeping rates. Furthermore, the subthreshold swing (SS) reaches the theoretical limit of kT/e ln (10) = 50 mV/decade at T = 250 K corresponding to a gate efficiency of ~1. Such a high gate efficiency can be attributed to the large electric-double-layer capacitance of the IL gate. The near ideal subthreshold swing also further indicates that the IL gate creates highly transparent tunneling contacts.[39]

To extract the carrier mobility, we first estimated the IL gate capacitance by measuring I_{ds} *versus* V_{ILg} of the same trilayer device at various fixed back-gate voltages, as shown in Figure 4b. As the back-gate

voltage is stepped up from the 0 to 30 V, the threshold voltage V_{th} of the $I_{ds}-V_{lLg}$ curves systematically shifts in the negative V_{lLg} direction, while the slope of the $I_{ds}-V_{lLg}$ curves remains nearly constant in the linear region. The small crossover between the $I_{ds}-V_{lLg}$ curve measured at V_{bg} = 30 V and corresponding measurements at lower back-gate voltages may be due to the hysteretic effect. The IL gate capacitance per unit area is estimated to be $C_{lLg} \sim 1.55 \times 10^{-6}$ F cm^{-2}. This estimate is based on the observed change of the threshold voltage ΔV_{th} in response to the change of the back-gate voltage ΔV_{bg} using the relationship $C_{lLg}/C_{bg} = \Delta V_{bg}/\Delta V_{th}$. We used $C_{bg} = 1.2 \times 10^{-8}$ F cm^{-2} for the capacitance per unit area between the channel and the back gate and the value $\Delta V_{bg}/\Delta V_{th}$ = 129, determined from the linear fit shown in the inset of Figure 4b. Using the expression $\mu = L/W \times dI_{ds}/dV_{lLg}/(C_{lLg}V_{ds})$, we estimated the low-field field-effect mobility of ~293 cm^2 V^{-1} s^{-1} using L = 3.3 μm for the channel length and W = 1.0 μm for the channel width, dI_{ds}/dV_{tg} for the slope of $I_{ds}-V_{lLg}$ curve in the linear region at V_{bg} = 0 V, and C_{lLg} ~1.55 × 10^{-6} F/cm^{-2}. Note that the value $C_{lLg} \sim 1.55 \times 10^{-6}$ F/cm^{-2} is about 4−5 times smaller than the C_{lLg} value determined by Hall measurements ($C_{lLg,H} \sim 7.2 \times 10^{-6}$ F cm^{-2}) on much thicker MoS_2 flakes.[32] The discrepancy may arise from the dependence of the quantum capacitance on the carrier density. The total capacitance C_{lLg}, consisting of the electrostatic capacitance C_e of the electric double layer and the quantum capacitance C_q of the MoS_2 channel, which are connected in series ($1/C_{lLg} = 1/C_e+1/C_q$). C_{lLg}, is likely dominated by C_q due to the extremely large electrostatic capacitance of the DEME-TFSI IL gate,[31] which can be as high as 100 μF/cm^2. Because C_q is a measure of the average density of states (DOS) at the Fermi level, which increases with increasing carrier density, the value of C_q may also increase with the carrier density.[10] As a result, the C_q is expected to be smaller in the low carrier density region near the threshold voltage than in the higher carrier density region [above $n_{2D} \sim 1 \times 10^{13}$ cm^2, as determined from $n_{2D} = C_{lLg,H}(V_{lLg,H} - V_{th})$], where the field-effect mobility is determined. This may lead to a possible underestimate of the total capacitance and thus an overestimate of the mobility. Using the capacitance $C_{lLg,H}$ = 7.2 μF cm^{-2}, determined by Hall measurement in multilayer flakes (>10 nm) at high carrier densities, the low limit of the field-effect mobility in our IL-gated trilayer MoS_2 device is determined to be 63 cm^2 V^{-1} s^{-1}, consistent with the Hall mobility measured in IL-gated MoS_2 multilayer flakes and with the mobility of multilayer MoS_2 on SiO_2 measured in a four-probe configuration.[32,40] We conclude that the actual extrinsic field-effect mobility lies likely between 63 cm^2 V^{-1} s^{-1} and 293 cm^2 V^{-1} s^{-1}, which is 1−2 orders of magnitude higher than the mobility observed in typical Si-back-gated monolayer and few-layer MoS_2 FETs. This indicates the reported mobility ranging between 0.1−10 cm^2 V^{-1} s^{-1} in monolayer and few-layer MoS_2 FETs has been largely limited by the contact resistance.[12,18,22]

It is also worth noting that our IL-gated MoS_2 channel is in a highly electron-doped state with a threshold voltage of $V_{th} \approx 0.5$ V at V_{lLg} = 0 V, which may be attributed to a higher concentration of positive than negative ions adsorbed in the vicinity of MoS_2. A large negative threshold voltage shift was also observed in high-κ dielectric passivated monolayer and multiplayer MoS_2 FETs, which could be attributed to the presence of a large amount of fixed positive charges in the dielectric layer, which have likely accumulated during the low temperature atomic layer deposition process.[22,23] Similar to the molecular ions adsorbed on the MoS_2 surface in IL-gated devices, these fixed charges in the thin high-κ dielectric layer could also reduce the Schottky barrier thickness and, thus, contribute to the reported mobility enhancement. Also, in carbon nanotube FETs, modest surface molecular doping has been shown to significantly reduce the Schottky barrier thickness, leading to a substantially enhanced tunneling current.[41]

To elucidate the transport mechanisms in the few-layer MoS_2 channel that was electrostatically doped by the IL, we measured the $I_{ds}-V_{bg}$ relationship in a different MoS_2 device (3.3 nm or 5 layers thick) between 77 and 180 K, after the device had been quickly cooled from 250 to 77 K at a fixed V_{lLg} = 0 V. Below the freezing point of the IL (≈200 K), the carrier charge density induced by the presence of positive ions, which preferentially enriched the vicinity of MoS_2, remained practically constant. The carefully chosen value V_{lLg} = 0 V of the IL-gate voltage allowed the creation of highly transparent tunneling contacts due to the adsorption of positive ions (implying n-doping), while the carrier density in the MoS_2 channel was kept low enough to allow an efficient reduction to zero by the back gate (see Figure 5a). As shown in the inset of Figure 5a, the $I_{ds}-V_{ds}$ characteristics are highly linear in the entire V_{ds} and V_{bg} range even at 77 K, indicating highly transparent contacts with thin Schottky barriers. To confirm that it is the electrostatic surface doping that is responsible for the drastic reduction of the contact resistance, we compared the device characteristics before the IL was added and after it was removed, following the completion of all electrical measurements. We observed nearly identical output characteristics in both cases (data not shown). Consequently, we may exclude the possibility of electrochemical doping or any other type of irreversible electrochemically induced degradation of the MoS_2 channel.

To avoid possible complications arising from the interplay between the IL gate and the back gate, we performed $I_{ds}-V_{bg}$ measurements only at temperatures below the freezing temperature of the IL in order

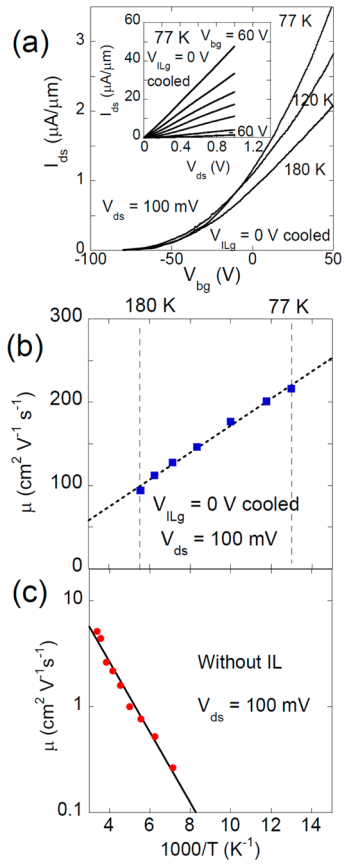


Figure 5. (a) Transfer curves of a 3.3 nm thick (5 layer) MoS_2 FET measured in the back-gate configuration with the drain-source bias V_{ds} = 100 mV and the IL-gate voltage kept at 0 V. The observations in the temperature range between 77 and 180 K were performed after the device had been cooled down from 250 to 77 K. The inset in (a) shows the output characteristics of the device measured at back-gate voltages between −60 and 60 V at T = 77 K. (b) Temperature dependence of the field-effect mobility extracted from the transfer characteristics in (a). (c) Temperature dependence of the field-effect mobility of the same device before the IL was added.

to suppress changes in the capacitance between the back-gate and the MoS_2 channel. In our previous study of polymer-electrolyte-gated monolayer-thick MoS_2 FETs, we attributed the beneficial influence of the polymer-electrolyte gate on the $I_{ds}-V_{bg}$ curves to a significant improvement of the carrier mobility.[42] However, the extent of mobility enhancement was overestimated by neglecting the additional IL capacitance that was induced by the back-gate voltage. In addition, capacitive coupling between the back and top gates through the large top-gate bonding pad may also lead to a significant underestimate of the back-gate capacitance in conventional dual-gated FET devices,[24] thus, causing a nominal overestimate of the mobility. Unlike in conventional top-gated (or dual-gated) devices, where the top-gate electrode is directly on top of the channel, inducing capacitive coupling, the metal gate electrode used in the IL gate, shown in Figure 1a, is located within the plane of the device and separated by several tens of micrometers, causing no change in the capacitance. As a result, the IL-gate electrode in our devices is capacitively decoupled from the transport channel and the back-gate in the temperature range between 77 and 180 K, ruling out the possibility of any stray capacitance arising from the gate electrode that may inadvertently cause a nominal increase in the back-gate capacitance. Our $I_{ds}-V_{bg}$ measurements with a floating and grounded IL gate, shown in Figure 5a, yield identical results, indicating that the IL-gate electrode has no effect on the back-gate capacitance when the IL is frozen.

Figure 5b,c shows the temperature dependence of the low-field field-effect mobility extracted from the $I_{ds}-V_{bg}$ curves in Figure 5a. These data are compared to the expected mobility in the same device with no IL present using the expression $\mu = L/W \times dI_{ds}/dV_{bg}/(C_{bg}V_{ds})$. For this estimate, we used L = 4.5 μm, W = 0.7 μm, and $C_{bg} = 1.2 \times 10^{-8}$ F cm^{-2} for the back-gate capacitance. The field-effect mobility with no IL present was observed to decrease from 5 cm^2 V^{-1} s^{-1} to 0.3 cm^2 V^{-1} s^{-1} as the temperature decreased from 295 to 140 K, following a simple activation temperature dependence depicted in Figure 5c. In this case, the mobility decreases much more rapidly than if it were limited by scattering from charged impurities.[43] This suggests that the charge transport behavior is largely limited by the Schottky barriers at the contacts and does not reflect the intrinsic behavior of the carrier mobility. We can extract an effective Schottky barrier height of $\Phi \sim 66$ meV from the temperature dependence of the extrinsic mobility $\mu \sim \exp(-\Phi/k_BT)$ in Figure 5c. This is lower than published theoretical estimates for an ideal interface,[25] possibly due to band bending induced by an applied gate voltage. In sharp contrast to this behavior, the mobility in presence of the IL gate increases from ~100 cm^2 V^{-1} s^{-1} to ~220 cm^2 V^{-1} s^{-1} as the temperature decreases from 180 to 77 K at a carrier concentration between 7×10^{12} and $<9 \times 10^{12}$ cm^{-2} [determined from $n_{2D} = C_{bg}(V_{bg}-V_{th})$], following a $\mu \sim T^{-\gamma}$ dependence with $\gamma \approx 1$. We conclude that in this case, the mobility is limited by the intrinsic behavior of the channel. Of course, dielectric screening in the IL gate could nominally increase the capacitive coupling.[43] Still, the observed qualitative change from thermally activated to "metallic" behavior caused by an IL gate, which acts as a top dielectric layer below the melting temperature, cannot be simply attributed to a possible underestimation of the back-gate capacitance. Extrapolating the $\mu \sim T^{-\gamma}$ fit with $\gamma \approx 1$ to the temperature T = 250 K yields a mobility value of $\mu \approx 70$ cm^2 V^{-1} s^{-1}, in good agreement with the mobility measured in the IL-gate configuration at 250 K. This provides further evidence that the mobility measured in the back gate configuration is unlikely an artifact due to the underestimation of back gate capacitance. Moreover, as discussed

in more detail below, our four-terminal measurements on a similar MoS_2 device show that the presence of the frozen IL, which forms an additional dielectric layer on top of the devices, does not substantially change the capacitance of the back-gate measurements.

Low-field field-effect channel mobility in this temperature range is affected by various scattering mechanisms, including scattering by acoustic and optical phonons, as well as long-range and short-range disorder that is present both in the bulk and near the surfaces of the channel. Kaasbjerg *et al.* showed theoretically that the mobility due to acoustic and optical phonon scattering in monolayer MoS_2 increases with decreasing temperature following a $\mu \sim T^{-\gamma}$ dependence, where the exponent γ depends on the dominant scattering mechanism.[44] At relatively low temperatures (<100 K), acoustic phonon scattering dominates, resulting in $\gamma = 1$. At higher temperatures, optical phonon scattering starts to dominate, and the exponent $\gamma > 1$ should cause a stronger temperature dependence of the mobility. On the other hand, the disorder-limited mobility decreases with decreasing temperature.[44,45] In our few-layer devices, the observed exponent ($\gamma \approx 1$) in the expression $\mu \sim T^{-\gamma}$ for the temperature dependence of the mobility coincides with that of transport dominated by acoustic-phonon scattering. In this case, however, the mobility values are substantially lower than what would be expected from acoustic-phonon-limited mobility, and the temperature was high enough to excite not only acoustic, but also optical phonons. This behavior can be understood in a likely scenario, where the top IL dielectric quenches phonon modes and thus reduces the γ value.

To verify that the extrinsic mobility of our IL-gated MoS_2 FETs approaches the true channel mobility, we also performed four-terminal measurements. An AFM image of the four-terminal device is shown in the inset of Figure 6a. We measured the conductance $G = I_{ds}/V_{inner}$, where V_{inner} is the potential difference across the voltage probes, at a fixed drain-source bias while sweeping the back-gate voltage. V_{inner} is kept below 70 mV during the measurement. Figure 6a shows the conductance *versus* back-gate voltage of an 8 nm thick MoS_2 flake measured at various temperatures, with a back-gate voltage of up to $V_{bg} = 70$ V. Under these conditions, we expect a charge carrier concentration of $n_{2D} = C_{bg}(V_{bg} - V_{th}) \sim 6.8 \times 10^{12}$ cm^{-2} at $V_{bg} = 70$ V, where the threshold voltage $V_{th} \approx -20$ V. The field-effect mobility can be extracted from the G *vs* V_{bg} curves in the $60 < V_{bg} < 70$ V range using the expression $\mu = L_{inner}/W \times (1/C_{bg}) \times dG/dV_{bg}$, where $L = 3.0\ \mu$m is the distance between the two voltage probes, $W = 5.0\ \mu$m, and $C_{bg} = 1.2 \times 10^{-8}$ F cm^{-2} is the back-gate capacitance. The steps in the conductance may be caused by the back-gate tuning of the voltage contacts. The voltage electrodes are very wide in our geometry, and their separation is only about twice their width.

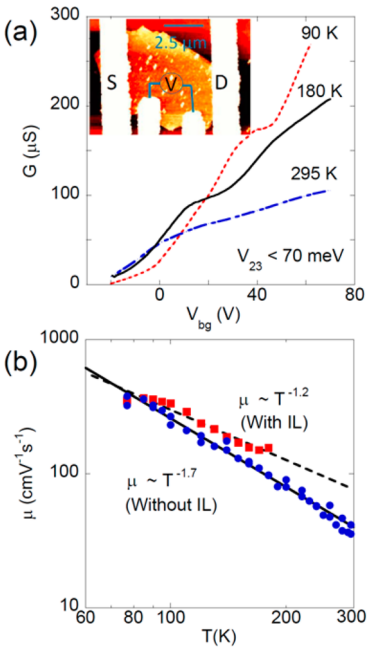


Figure 6. Four-terminal electron transport in a back-gated 8 nm thick MoS_2 FET with and without IL. (a) Conductance as a function of back-gate voltage measured at different temperatures with no IL present. The inset shows an AFM image of the four-terminal device. (b) Temperature dependence of the true channel mobility derived from the four-terminal measurements in presence and absence of the IL.

In this case, the effective distance between them may change with applied gate-voltage. Figure 6b shows the temperature dependence of the true channel mobility with and without the frozen IL as a dielectric capping layer. Before the IL was added, we observed a mobility increase from ≈40 cm^2 V^{-1} s^{-1} at 300 K to ≈390 cm^2 V^{-1} s^{-1} at 77 K following a $\mu \sim T^{-\gamma}$ dependence with $\gamma \approx 1.7$ in the entire temperature range, in good agreement with theoretical predictions for an MoS_2 monolayer.[44] Although our 8 nm thick sample is much thicker than a monolayer, back-gating has the strongest effect on the bottom MoS_2 layers. Moreover, charge screening also reduces the number of charge carriers in the top layers, especially at high back-gate voltages.[27,46] The relatively low overall mobility values in this device may be attributed to additional extrinsic scattering mechanisms such as impurity scattering and scattering off surface polar optical phonons of the SiO_2 gate dielectric.[44] Interestingly, the overall mobility of the device with the IL is similar to that without the IL in the temperature range between 77 and 180 K, indicating that the IL as a capping top dielectric does not substantially impact the back gate capacitive coupling when it is frozen. On the other hand, the temperature dependence of the mobility weakens upon adding the IL, following a $\mu \sim T^{-\gamma}$ dependence with $\gamma \approx 1.2$ for $77 < T < 180$ K. This weaker temperature dependence of the channel mobility μ in presence of IL dielectric capping is consistent with that of the extrinsic mobility shown in Figure 5b, which can be attributed to phonon mode quenching

caused by the IL dielectric.[43] Note that the extrinsic mobility values in Figure 5b, which include the contact resistance, are in good agreement with the true channel mobility values in Figure 6b. This is a further demonstration that IL gating effectively creates highly transparent electrical contacts and reveals the intrinsic channel-limited device properties of MoS_2 FETs. This finding shows that the previously reported low mobility of Si-back-gated MoS_2 FETs, ranging typically between 0.1 – 10 $cm^2 V^{-1} s^{-1}$, may not represent the intrinsic channel property, but was rather limited by nonideal contacts, as pointed out by Popov *et al.*[25] It also demonstrates that phonon-limited mobility can be achieved without substantially reducing the disorder near the channel/dielectric interface.

Since the carriers induced by the IL gate are close to the top surface of the MoS_2 channel, the interface properties in these devices may be different from back-gated devices with no IL, where the carriers are closer to the bottom surface. To rule out the possibility that the drastic difference in mobility between MoS_2 devices with and without an IL gate arises from differences at the channel/dielectric interface, we measured another few-nanometer thick (5 nm or ~7 layers) back-gated MoS_2 with patterned *n*-doping. As shown in the inset of Figure 7a, both the electrical contacts and a small section of the channel near each electrode are covered by a 50 nm thick layer of positive resist (hydrogen silsesquioxane, HSQ), defined by standard electron beam lithography at a dose of 200 $\mu C/cm^2$, while the large portion of the channel is not covered by HSQ. At low degrees of cross-linking obtained at low electron beam dosages, Si–H bonds in HSQ are readily broken and release hydrogen, increasing electron density in MoS_2 near the contacts.[47] Consequently, HSQ covered contact regions are *n*-doped, while the bare channel region remains undoped. Figure 7a shows selected transfer curves of the back-gated device at temperatures between 77 and 295 K, from which the field-effect mobility can be extracted. As shown in Figure 7b, the mobility increases from ~75 $cm^2 V^{-1} s^{-1}$ to ~180 $cm^2 V^{-1} s^{-1}$ as the temperature drops from 295 to 140 K, suggesting that mobility in this temperature range is largely limited by phonon scattering. Below 140 K, the mobility starts decreasing with decreasing temperature, which can be attributed to the reduction of the thermally assisted tunneling current through a Schottky barrier. Because the main difference between this device and other back-gated, few-nanometer-thick MoS_2 FETs is the *n*-doping of the contacts, the observed high mobility at room temperature and its phonon-limited temperature dependence above 140 K can be attributed to the Schottky barrier thinning by the surface doping in the contact regions, which is albeit not as effective as IL gating. The slightly lower mobility in the IL-gated device (Figure 5b) than in the HSQ contact-doped device (Figure 7b) above 140 K

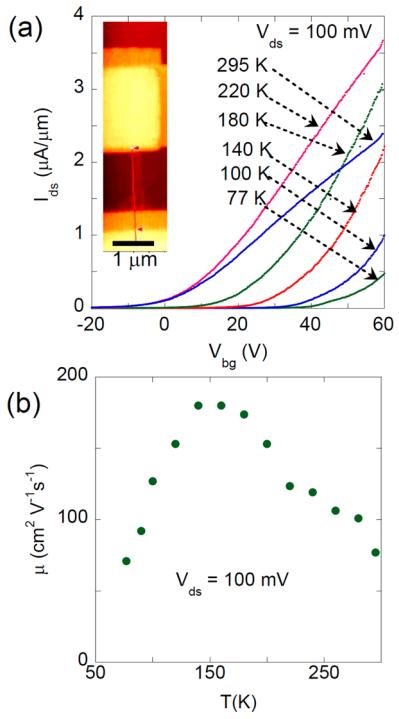


Figure 7. (a) Transfer characteristics of a back-gated 5 nm thick MoS_2 FET measured at the drain-source bias V_{ds} = 100 mV, for various temperatures. The inset of (a) shows an AFM image of the device with its electrical contacts covered by HSQ, while a large portion of the channel is bare. (b) Field-effect mobility of the device as a function of temperature.

may be attributed to the presence of added charge impurities from the IL.[48] This finding unambiguously demonstrates that the observed mobility enhancement in IL-gated MoS_2 FETs is not an interface effect and cannot be simply attributed to the reduction of charge scattering in the transport channel.

CONCLUSIONS

In conclusion, we report the fabrication of IL-gated MoS_2-based field-effect transistors with significantly higher mobilities than reported in comparable back-gated devices. We attribute the observed mobility enhancement to the IL, which acts as an ultrathin dielectric that effectively reduces the Schottky barrier thickness at the MoS_2/metal contacts by strong band-bending. The substantially reduced contact resistance in IL-gated bilayer and few-layer MoS_2 FETs results in an ambipolar behavior with high ON/OFF ratios, a near-ideal subthreshold swing, and significantly improved field-effect mobility. Remarkably, the mobility of a 3 nm thick MoS_2 FET with IL-gating was found to increase from ~100 $cm^2 V^{-1} s^{-1}$ to ~220 $cm^2 V^{-1} s^{-1}$ as the temperature decreased from 180 to 77 K. This finding is in quantitative agreement with the true channel mobility measured by four-terminal measurement, suggesting that the mobility is predominantly limited by phonon-scattering. It is remarkable that the high mobility has not been degraded by the presence of

both long-range disorder (e.g., from charged impurities) and short-range disorder (e.g., interface roughness scattering) at the MoS_2/SiO_2 and MoS_2/IL interface. The effect of Schottky barrier thinning on the performance of MoS_2 FETs was further verified by patterned *n*-doping of the contact regions using HSQ. More detailed studies of MoS_2 FETs with HSQ doped contacts are underway. Our study of IL-gated MoS_2 FETs clearly demonstrates that previously observed low mobility values in monolayer and few-layer MoS_2 devices were largely caused by the large contact resistance. We found that phonon-limited mobility can be recovered through Schottky barrier thinning even in the presence of nonideal channel/dielectric interfaces. We also surmise that the reported drastic mobility improvement in high-κ dielectric-capped MoS_2 FETs may be partially attributed to the Schottky barrier thinning caused by the doping of the fixed charges in the thin dielectric layer in addition to dielectric screening.

METHOD

Atomically thin MoS_2 flakes were produced by repeated splitting of a bulk crystal using a mechanical cleavage method and subsequently transferred onto degenerately doped silicon substrates covered with a 290 nm thick thermal oxide layer. An optical microscope was used to identify thin flakes, which were further characterized by Park-Systems XE-70 noncontact mode atomic force microscopy (AFM). MoS_2 IL-FET devices were fabricated by first patterning the source, drain, and gate electrodes, consisting of 5 nm of Ti covered by 50 nm of Au, using standard electron beam lithography and electron beam deposition. A small droplet of the DEME-TFSI IL (Sigma Aldrich 727679) was then carefully applied onto the devices using a micromanipulator under an optical microscope, covering the MoS_2 layer and the source, drain, and gate electrodes. The IL gate forms by self-assembly. Electrical properties of the devices were measured by a Keithley 4200 semiconductor parameter analyzer in a Lakeshore Cryogenic probe station after dehydrating the IL under high vacuum ($\sim 1 \times 10^{-6}$ Torr) for 48 h.

Conflict of Interest: The authors declare no competing financial interest.

Acknowledgment. This work was supported by NSF (No. ECCS-1128297). D.T. was supported by the National Science Foundation Cooperative Agreement No. EEC-0832785, titled "NSEC: Center for High-rate Nanomanufacturing." Part of this research was conducted at the Center for Nanophase Materials Sciences under Project No. CNMS2011-066. The authors also thank Michael Fuhrer and Kristen Kaasbjerg for helpful discussion.

REFERENCES AND NOTES

1. Balandin, A. A.; Ghosh, S.; Bao, W.; Calizo, I.; Teweldebrhan, D.; Miao, F.; Lau, C. N. Superior Thermal Conductivity of Single-Layer Graphene. *Nano Lett.* **2008**, *8*, 902–907.
2. Ghosh, S.; Calizo, I.; Teweldebrhan, D.; Pokatilov, E. P.; Nika, D. L.; Balandin, A. A.; Bao, W.; Miao, F.; Lau, C. N. Extremely High Thermal Conductivity of Graphene: Prospects for Thermal Management Applications in Nanoelectronic Circuits. *Appl. Phys. Lett.* **2008**, *92*, 151911.
3. Seol, J. H.; Jo, I.; Moore, A. L.; Lindsay, L.; Aitken, Z. H.; Pettes, M. T.; Li, X.; Yao, Z.; Huang, R.; Broido, D.; et al. Two-Dimensional Phonon Transport in Supported Graphene. *Science* **2010**, *328*, 213–216.
4. Bolotin, K. I.; Sikes, K. J.; Jiang, Z.; Klima, M.; Fudenberg, G.; Hone, J.; Kim, P.; Stormer, H. L. Ultrahigh Electron Mobility in Suspended Graphene. *Solid State Commun.* **2008**, *146*, 351–355.
5. Ponomarenko, L. A.; Schedin, F.; Katsnelson, M. I.; Yang, R.; Hill, E. W.; Novoselov, K. S.; Geim, A. K. Chaotic Dirac Billiard in Graphene Quantum Dots. *Science* **2008**, *320*, 356–358.
6. Son, Y.-W.; Cohen, M. L.; Louie, S. G. Energy Gaps in Graphene Nanoribbons. *Phys. Rev. Lett.* **2006**, *97*, 216803.
7. Ming-Wei, L.; Ling, C.; Zhang, Y.; Yoon, H. J.; Cheng, M. M.-C.; Agapito, L.; Kioussis, N.; Widjaja, N.; Zhou, Z. Room-Temperature High On/Off Ratio in Suspended Graphene Nanoribbon Field-Effect Transistors. *Nanotechnology* **2011**, *22*, 265201.
8. Lin, M.-W.; Ling, C.; Agapito, L. A.; Kioussis, N.; Zhang, Y.; Cheng, M. M.-C.; Wang, W. L.; Kaxiras, E.; Zhou, Z. Approaching the Intrinsic Band Gap in Suspended High-Mobility Graphene Nanoribbons. *Phys. Rev. B* **2011**, *84*, 125411.
9. Zhang, Y.; Tang, T.-T.; Girit, C.; Hao, Z.; Martin, M. C.; Zettl, A.; Crommie, M. F.; Shen, Y. R.; Wang, F. Direct Observation of a Widely Tunable Bandgap in Bilayer Graphene. *Nature* **2009**, *459*, 820–823.
10. Yoon, Y.; Ganapathi, K.; Salahuddin, S. How Good Can Monolayer MoS_2 Transistors Be? *Nano Lett.* **2011**, *11*, 3768–3773.
11. Mak, K. F.; Lee, C.; Hone, J.; Shan, J.; Heinz, T. F. Atomically Thin MoS_2: A New Direct-Gap Semiconductor. *Phys. Rev. Lett.* **2010**, *105*, 136805.
12. Novoselov, K. S.; Jiang, D.; Schedin, F.; Booth, T. J.; Khotkevich, V. V.; Morozov, S. V.; Geim, A. K. Two-Dimensional Atomic Crystals. *Proc. Natl. Acad. Sci. U.S.A.* **2005**, *102*, 10451–10453.
13. Gourmelon, E.; Lignier, O.; Hadouda, H.; Couturier, G.; Bernède, J. C.; Tedd, J.; Pouzet, J.; Salardenne, J. MS_2 (M = W, Mo) Photosensitive Thin Films for Solar Cells. *Sol. Energy Mater. Sol. Cells* **1997**, *46*, 115–121.
14. Zong, X.; Yan, H.; Wu, G.; Ma, G.; Wen, F.; Wang, L.; Li, C. Enhancement of Photocatalytic H_2 Evolution on Cds by Loading MoS_2 as Cocatalyst under Visible Light Irradiation. *J. Am. Chem. Soc.* **2008**, *130*, 7176–7177.
15. Takahashi, T.; Takenobu, T.; Takeya, J.; Iwasa, Y. Ambipolar Light-Emitting Transistors of a Tetracene Single Crystal. *Adv. Funct. Mater.* **2007**, *17*, 1623–1628.
16. Yin, Z.; Li, H.; Li, H.; Jiang, L.; Shi, Y.; Sun, Y.; Lu, G.; Zhang, Q.; Chen, X.; Zhang, H. Single-Layer MoS_2 Phototransistors. *ACS Nano* **2012**, *6*, 74–80.
17. Wang, H.; Yu, L.; Lee, Y.-H.; Shi, Y.; Hsu, A.; Chin, M. L.; Li, L.-J.; Dubey, M.; Kong, J.; Palacios, T. Integrated Circuits Based on Bilayer MoS_2 Transistors. *Nano Lett.* **2012**, *12*, 4674–4680.
18. Ghatak, S.; Pal, A. N.; Ghosh, A. Nature of Electronic States in Atomically Thin MoS_2 Field-Effect Transistors. *ACS Nano* **2011**, *5*, 7707–7712.
19. Li, H.; Yin, Z.; He, Q.; Li, H.; Huang, X.; Lu, G.; Fam, D. W. H.; Tok, A. I. Y.; Zhang, Q.; Zhang, H. Fabrication of Single- and Multilayer MoS_2 Film-Based Field-Effect Transistors for Sensing NO at Room Temperature. *Small* **2012**, *8*, 63–67.
20. Fivaz, R.; Mooser, E. Mobility of Charge Carriers in Semiconducting Layer Structures. *Phys. Rev.* **1967**, *163*, 743–755.
21. Liu, H.; Neal, A. T.; Ye, P. D. Channel Length Scaling of MoS_2 MOSFETs. *ACS Nano* **2012**, *6*, 8563–8569.
22. Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-Layer MoS_2 Transistors. *Nat. Nanotechnol.* **2011**, *6*, 147–150.
23. Liu, H.; Ye, P. D. MoS_2 Dual-Gate MOSFET with Atomic-Layer-Deposited Al_2O_3 as Top-Gate Dielectric. *IEEE Electron Dev. Lett.* **2012**, *33*, 546–548.
24. Fuhrer, M. S.; Hone, J. Measurement of Mobility in Dual-Gated MoS_2 Transistors. *Condens. Matter* **2013**, submitted for publication, Arxiv:1301.4288.

25. Popov, I.; Seifert, G.; Tománek, D. Designing Electrical Contacts to MoS_2 Monolayers: A Computational Study. *Phys. Rev. Lett.* **2012**, *108*, 156802.
26. Lee, K.; Kim, H.-Y.; Lotya, M.; Coleman, J. N.; Kim, G.-T.; Duesberg, G. S. Electrical Characteristics of Molybdenum Disulfide Flakes Produced by Liquid Exfoliation. *Adv. Mater.* **2011**, *23*, 4178–4182.
27. Das, S.; Chen, H.-Y.; Penumatcha, A. V.; Appenzeller, J. High Performance Multilayer MoS_2Transistors with Scandium Contacts. *Nano Lett.* **2012**, *13*, 100–105.
28. Fang, H.; Chuang, S.; Chang, T. C.; Takei, K.; Takahashi, T.; Javey, A. High-Performance Single Layered WSe_2 P-Fets with Chemically Doped Contacts. *Nano Lett.* **2012**, *12*, 3788–3792.
29. Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A. Electric Field Effect in Atomically Thin Carbon Films. *Science* **2004**, *306*, 666–669.
30. Cheng, L.; Setzler, G.; Lin, M.-W.; Dhindsa, K.; Jin, J.; Yoon, H. J.; Kim, S. S.; Cheng, M. M.-C.; Widjaja, N.; Zhou, Z. Electrical Transport Properties of Graphene Nanoribbons Produced from Sonicating Graphite in Solution. *Nanotechnology* **2011**, *22*, 325201.
31. Yuan, H.; Shimotani, H.; Tsukazaki, A.; Ohtomo, A.; Kawasaki, M.; Iwasa, Y. Hydrogenation-Induced Surface Polarity Recognition and Proton Memory Behavior at Protic-Ionic-Liquid/Oxide Electric-Double-Layer Interfaces. *J. Am. Chem. Soc.* **2010**, *132*, 6672–6678.
32. Zhang, Y.; Ye, J.; Matsuhashi, Y.; Iwasa, Y. Ambipolar MoS_2 Thin Flake Transistors. *Nano Lett.* **2012**, *12*, 1136–1140.
33. Pachoud, A.; Jaiswal, M.; Ang, P. K.; Loh, K. P.; Özyilmaz, B. Graphene Transport at High Carrier Densities Using a Polymer Electrolyte Gate. *Europhys. Lett.* **2010**, *92*, 27001.
34. Ye, J. T.; Zhang, Y. J.; Akashi, R.; Bahramy, M. S.; Arita, R.; Iwasa, Y. Superconducting Dome in a Gate-Tuned Band Insulator. *Science* **2012**, *338*, 1193–1196.
35. Ji, H.; Wei, J.; Natelson, D. Modulation of the Electrical Properties of VO_2 Nanobeams Using an Ionic Liquid as a Gating Medium. *Nano Lett.* **2012**, *12*, 2988–2992.
36. Svensson, J.; Campbell, E. E. B. Schottky Barriers in Carbon Nanotube-Metal Contacts. *J. Appl. Phys.* **2011**, *110*, 111101.
37. Braga, D.; Gutiérrez Lezama, I.; Berger, H.; Morpurgo, A. F. Quantitative Determination of the Band Gap of WS_2 with Ambipolar Ionic Liquid-Gated Transistors. *Nano Lett.* **2012**, *12*, 5218–5223.
38. Late, D. J.; Liu, B.; Matte, R. H. S. S.; Dravid, V. P.; Rao, C. N. R. Hysteresis in Single-Layer MoS_2 Field Effect Transistors. *ACS Nano* **2012**, *6*, 5635–5641.
39. Siddons, G. P.; Merchin, D.; Back, J. H.; Jeong, J. K.; Shim, M. Highly Efficient Gating and Doping of Carbon Nanotubes with Polymer Electrolytes. *Nano Lett.* **2004**, *4*, 927–931.
40. Bao, W.; Cai, X.; Kim, D.; Sridhara, K.; Fuhrer, M. S. High Mobility Ambipolar MoS_2 Field-Effect Transistors: Substrate and Dielectric Effects. *Condens. Matter* **2012**, submitted for publication, arXiv:1212.6292v1.
41. Chen, Y.-F.; Fuhrer, M. S. Tuning from Thermionic Emission to Ohmic Tunnel Contacts *via* Doping in Schottky-Barrier Nanotube Transistors. *Nano Lett.* **2006**, *6*, 2158–2162.
42. Lin, M.-W.; Liu, L.; Lan, Q.; Tan, X.; Dhindsa, K.; Zeng, P.; Naik, V. M.; Cheng, M. M.-C.; Zhou, Z. Mobility Enhancement and Highly Efficient Gating of Monolayer MoS_2 Transistors with Polymer Electrolyte. *J. Phys. D: Appl. Phys.* **2012**, *45*, 345102.
43. Radisavljevic, B.; Kis, A. Mobility Engineering and Metal-Insulator Transition in Monolayer MoS_2. *Condens. Matter* **2012**, submitted for publication, arXiv:1301.4947v1.
44. Kaasbjerg, K.; Thygesen, K. S.; Jacobsen, K. W. Phonon-Limited Mobility in N-Type Single-Layer MoS_2 from First Principles. *Phys. Rev. B* **2012**, *85*, 115317.
45. Kim, S.; Konar, A.; Hwang, W.-S.; Lee, J. H.; Lee, J.; Yang, J.; Jung, C.; Kim, H.; Yoo, J.-B.; Choi, J.-Y.; et al. High-Mobility and Low-Power Thin-Film Transistors Based on Multilayer MoS_2 Crystals. *Nat. Commun.* **2012**, *3*, 1011.
46. Das, S.; Appenzeller, J. Screening and Interlayer Coupling in Multilayer MoS_2. *Phys. Status Solidi* **2013**, *7*, 268–273.
47. Brenner, K.; Murali, R. Single Step, Complementary Doping of Graphene. *Appl. Phys. Lett.* **2010**, *96*, 063104.
48. Das, A.; Pisana, S.; Chakraborty, B.; Piscanec, S.; Saha, S. K.; Waghmare, U. V.; Novoselov, K. S.; Krishnamurthy, H. R.; Geim, A. K.; Ferrari, A. C.; et al. Monitoring Dopants by Raman Scattering in an Electrochemically Top-Gated Graphene Transistor. *Nat. Nanotechnol.* **2008**, *3*, 210–215.